REMARKS

1-26 are pending in the application and stand rejected. In particular, the following obviousness rejections are asserted:

(i) Claims 1-6, 10-12, 16-24 and 26 are rejected as being unpatentable over Iyengar (U.S. Pat. Pub. No. 2003/0172236) in view of Hiraoka et al.(U.S. Patent No. 4,733,348); and

(ii) Claims 7-9, 14-15 and 25 are rejected as being unpatentable over Iyengar and Hiraoka and further in view of Chang (U.S. Pat. Pub. 2005/0128960).

Applicants contend that at the very least, claims 1, 10, 11, 17 and 18 are patentable and non-obvious over the combination of Iyengar and Hiraoka. For example, Applicants respectfully assert that the combination of Iyengar and Hiraoka do not disclose or fairly suggest a method for maintaining consistency of stored objects which includes, for example, performing an updating process by instructing storage elements that may be storing a copy of the object (to be updated) to invalidate their copy of the object and then *delaying an updating of the object until it is determined that each storage element instructed to invalidate a copy of the object has either (i) acknowledged that it is not storing a valid copy of the object or (ii) been deemed unresponsive*, as essentially claimed in claims 1, 10, 11, 17 and 18.

In formulating the rejections, the Examiner seemingly relies on Iyengar as generally disclosing that a central cache may communicate with local caches to make sure that copies of an object to be updated are invalidated. However, Iyengar does not specifically teach that updating of the object is *delayed until it is determined that each storage element instructed to invalidate a copy of the object has either (i) acknowledged*

that it is not storing a valid copy of the object or (ii) been deemed unresponsive, as recited in the claimed inventions. In fact, the Examiner acknowledges at the very least that Iyengar does not specifically disclose *delaying an updating of the object until it is determined that each storage element instructed to invalidate a copy of the object has . . . been deemed unresponsive.*

However, the Examiner seemingly relies on the teachings of Hiraoka in Col. 4, lines 41-50 as curing the deficiencies of Iyengar in this regard. But it is respectfully submitted that the Examiner's reliance on Hiraoka is wholly misplaced in this regard, as Hiraoka does not fairly teach or suggest *delaying an updating of the object until it is determined that each storage element instructed to invalidate a copy of the object has . . . been deemed unresponsive.*

In stark contrast, Hiraoka teaches a virtual memory control multiprocessor system having a plurality of processors each having a translation look aside buffer, including: purge request signal generating means for supplying a common purge request signal requesting purge operations of translation look aside buffers of other processors excluding a source processor for generating the common purge request signal which is supplied in parallel to the other processors; a plurality of flip-flops for storing, in units of processors, a purge end signal sent back from the other processors which complete purge operations in response to the common purge request signal generated from the purge request signal generating means; and purge end detecting means for checking the statuses of the plurality of flip-flops and detecting the end of purge operations of all processors (see. Col. 2, lines 3-21).

Hiraoka teaches that in a virtual memory control multiprocessor system, the purging (initialization) of TLBs of all process must be performed to equalize the contents of the TLBs (see Col. 1, lines 10-15).

In this regard, on a fundamental level, Hiraoka utterly fails to teach or suggest a system for instructing storage elements to invalidate a stored copy of an object, but rather Hiraoka is directed to a system for purging the contents of TLB (table look aside butters) of a set of parallel processors. The teachings of Hiraoka regarding the process for purging TLBs of a multiprocessor system are very much different and irrelevant to the systems and methods as contemplated by the claimed inventions for maintaining consistency of copies of an object stored in storage elements.

In fact, as noted above, Hiraoka teaches that initialization (purging) of all processors must be completed for at certain times for all processors. In this regard, there is nothing in Hiraoka that fairly teaches or suggests that the purging of one of the processors in a multiprocessor system can be skipped or disregarded (and subsequent tasks performed) in the event of a timeout condition (after issuance of a purge request signal) if one processor is unresponsive.

The Examiner relies on Col. 4, lines 41-50 of Hiraoka as teaching delaying updating until a processor is deemed unresponsive. However, Hiraoka teaches in Col. 4, lines 41-50 the following:

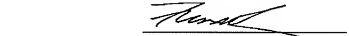
> The above operation can be performed when all the processors 20.sub.0 through 20.sub.3 are present. However, when the processor 20.sub.3 is not present, the following operation is performed. The signal 48.sub.3 representing that the processor 20.sub.3 is not present is set at logic "1". The signal 48.sub.3 of logic "1" is supplied to the OR gate 42.sub.3. The OR gate 42.sub.3 supplies the dummy TLB purge end signal to the AND gate 43. If the processor 20.sub.3 is not present, the processor

20.sub.0 can detect that all the TLB purge operations of the processors 20.sub.0 through 20.sub.2 are completed.

There is nothing in the cited paragraph relating to an unresponsive processor, but merely a condition in which the multiprocessor system comprise 3 processors instead of 4. As such, it is respectfully submitted that the Examiner's reliance on the cited passage is misplace.

In view of the above, claims 1, 10, 11, 17 and 18 include features that are not disclosed or suggested by Iyengar and Hiraoka, either singularly or in combination, and are thus, non-obvious over such combination. Given that all remaining obviousness rejections for those claims depending from independent claims 1, 10, 11, 17 and 18 are based directly or primarily on the combination of Iyengar and Hiraoka as applied to the independent claims, all obviousness rejections are legally deficient for at least the same reasons given above. Accordingly, withdrawal of the obviousness rejections is respectfully requested.

Respectfully submitted,



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